REMARKS

The Examiner rejected claims 1, 3-4, 8 and 10 under 35 U.S.C. §102(e) as being unpatentable over Lin et al. (US 6, 852,576).

The Examiner rejected claims 11-13, 15-16 and 18 under 35 U.S.C. §102(e) as being unpatentable over Yeo et al. (US 6, 867,433).

The Examiner rejected claims 2, 6-7 and 9 under 35 U.S.C. 103 as being unpatentable over Lin et al. in view of Yeo et al.

The Examiner rejected claims 17 and 19-21 under 35 U.S.C. 103 as being unpatentable over Yeo et al. in view of Lin et al.

The Examiner rejected claims 5 and 14 under 35 U.S.C. 103 as being unpatentable over Yeo et al. or Lin et al. in view of Buynoski et al. (6,709,982).

Applicants respectfully traverse the §102(e) and §103(a) rejections with the following arguments.

35 USC § 102

As to claim 1, the Examiner states that "Lin et al. teach in figures 1-9 and related text a method of forming an FinFET device, comprising: (a) providing a semiconductor substrate 200, (b) forming a dielectric layer on a top surface of said substrate (column 3, lines 6-8); (c) forming a silicon fin 410 on a top surface of said dielectric layer; (d) forming a protective layer 510 on at least one sidewall of said fin; and (e) removing said protective layer from said at least one sidewall in a channel region of said fin (column 4, lines 7-8). (f) forming a gate dielectric on exposed surfaces of said fin in said channel region; and (g) forming a conductive gate on said gate dielectric. (h) removing said protective layer from source/drain regions of said fin, wherein said fin has a height of about 500 to 2000A and has a width of about 200 to 500A, and wherein said fin comprises mono-crystalline silicon."

Applicants contend that claim 1, as amended, is not anticipated by Lin et al. because CITE does not teach each and every feature of claim 1. As a first example Lin et al. does not teach "forming a silicon layer on a top surface of said dielectric layer; forming a patterned hardmask on a top surface of said silicon layer; removing said silicon layer where said silicon layer is not protected by said patterned hardmask thereby forming a silicon fin having a top surface and sidewalls on a top surface of said dielectric layer"

Applicants respectfully point out that Lin et al. in FIG 2, forms silicon fins by: starting with a dielectric mandrel 210; in FIG. 3, forms a conformal silicon layer 310 over mandrel 210; in FIG. 4, converts the conformal layer to silicon spacers 410 which is an entirely different process than recited in Applicants claim 1.

As a second example, Lin et al. does not teach or suggest "removing said patterned hardmask and a less than whole portion of said dielectric layer from under said fin," as Lin et al.

has no hardmask to remove and does not remove any of substrate 200 from under fins 410. The Examiner had alleged that Buynoski et al. had taught removal of dielectric from under a silicon fin. Applicants respectfully maintain, the Examiner was in error. Applicants respectfully point out that element 620 is not "a portion of said dielectric layer 210" but is silicon as taught in Buynoski et al. col. 3, lines 34-37 which states "As illustrated in FIG. 6, the portion of silicon layer 220 below the remaining portions of oxide layer 230 are denoted as field silicon 620."

As a third example, Lin et al. does not teach or suggest "forming a conformal protective layer on at least one sidewall of said fin, said protective layer extending under said fin." Applicants point out layer 510 is not conformal (note layer 510 is thicker than the height of mandrel 210 or fin 410 and thus is not conformal) and does not extend under fins 410.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Lin et al. and is in condition for allowance. Since claims 2-4, 6-8, 10, 29 and 30 depend from claim 1, Applicants respectfully maintain that claims 2-4, 6-8, 10, 29 and 30 are likewise in condition for allowance.

As to claims 11 and 13, the Examiner states that "Yeo et al. teach in figure 12 and related text a method of forming an FinFET device, comprising: (a) providing a semiconductor substrate 204, (b) forming a dielectric layer 152 on a top surface of said substrate; (c) forming a silicon fin 155 having sidewalls on a top surface. of said dielectric layer; (d) forming a protective spacer layer 164 on at least one sidewall of said fin; and (e) performing at least one ion implantation step into said fin. (f) forming a gate dielectric 164 on exposed surfaces of said fin in said channel region;(g) forming a conductive gate 1610 on said gate dielectric, wherein said protective layer comprises tetraethoxysilane oxide or silicon nitride, and is about 15 to 50A thick, wherein step (c) comprises: forming a silicon layer 202 on said top surface of said dielectric layer 152 (figure

12a); forming a mask (not shown) over said silicon layer; removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and removing said mask."

Applicants contend that claim 11, as amended, is not anticipated by Yeo et al. because Yeo et al. does not teach each and every feature of claim 11. As a first example Yeo et al. does not teach "removing said patterned hardmask and a less than whole portion of said dielectric layer from under said fin."

Applicants point out that there is no removal of any portion of dielectric layer 152 taught by Yeo et al. and specifically no removal of dielectric layer 152 from under fin 155 (see Yeo et al. FIGs. 12a-12j).

As a second example, Yeo et al. does not teach or suggest "forming a protective spacer on at least a lower portion of at least one of said sidewalls, said protective spacer not extending to said top surface of said fin, said protective spacer extending under said silicon fin." Applicants point out that layer 164 of Yeo et al. extends to the top surface of fin 155 and does not extend under fin 155 (see Yeo et al. FIG. 12C).

Based on the preceding arguments, Applicants respectfully maintain that claim 11 is not unpatentable over Yeo et al. and is in condition for allowance. Since claims 12, 13, 15-17 and 21 depend from claim 11, Applicants respectfully maintain that claims 12, 13, 15-17 and 21 are likewise in condition for allowance.

Applicants contend that claim 11, as amended, is not anticipated by Yeo et al. because Yeo et al. does not teach each and every feature of claim 11. For example Yeo et al. does not teach "forming a gate dielectric on exposed surfaces of said fin in at least a channel region of said fin and over said protective spacer."

Applicants, note that the Examiner states that Yeo et al. element 164 is first a protective spacer *layer* and then a gate dielectric. Applicants point out that element 164 can not be on top of itself.

35 USC § 103 Rejections

As to claim 19, the Examiner states that "Lin et al. teach in figures 2-4 step (c) comprises: forming a mandrel 210 on said dielectric layer, depositing a conformal silicon layer 310 on a top surface and a sidewall of said mandrel and on surfaces of said dielectric layer not covered by said mandrel, removing said conformal silicon layer from said top surface of said mandrel and said surfaces of said dielectric layer not covered by said mandrel, and after the step of removing, performing a high temperature anneal of said conformal silicon layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form step (c) by the process of Lin et al.'s in Yeo et al.'s device in order to improve the device characteristics."

Applicants contend that claim 19, as amended, is not obvious in view of Yeo et al. in view of Lin et al. because Yeo et al. in view of Lin et al.does not teach or suggest every feature of claim 19. In a first example, Yeo et al. in view of Lin et al. does not teach or suggest "forming a protective spacer on a lower portion of said exposed sidewall of said silicon spacer, said protective spacer not extending to said top surface of said silicon spacer."

Applicants point out that neither Yeo et al. or Lin et al. teach two spacers having the physical/geometrical relationship claimed by Applicants.

In a second example, Yeo et al. in view of Lin et al. does not teach or suggest "removing said mandrel."

Applicants point out that Yeo et al, does not teach a mandrel and Liu et al. teaches not removing the mandrel.

Based on the preceding arguments, Applicants respectfully maintain that claim 19 is not unpatentable over Yeo et al. in view of Lin et al.and is in condition for allowance. Since claim

20 depends from claim 19, Applicants respectfully maintain that claim 20 is likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Anderson et al.

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